InnoDisk EDC4000

Embedded Disk Card 4000

Datasheet

Ver 1.1

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REVISION HISTORY

Revision	Description	Date
1.0	Release first version	December 2007
1.1	Modify storage temperature and release 8GB availability	April 2008

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1. Product Overview

1.1 Introduction to Embedded Disk Card 4000

Embedded Disk Card 4000 (EDC4000) products provide high capacity solid-state flash memory that electrically complies with the Personal Computer Memory Card International Association ATA standard. InnoDisk Embedded Disk Card 4000 (EDC4000) is embedded solid-state data storage systems for industrial work place. Embedded Disk Card 4000 (EDC4000) features an extremely light weight, reliable, low-profile form factor.

Embedded Disk Card 4000 (EDC4000) supports advanced PIO (0-4), Multi Word DMA (0-2), Ultra DMA (0-4) transfer modes, multi-sector transfers, and LBA addressing.

1.2 Product Models

Embedded Disk Card 4000 (EDC4000) is available in capacities ranging from 32MB to 8GB, making the upgrade path simple and fast.

Available in 40-pin and 44-pin horizontal connector packages, EDC4000 fits into any platform with an IDE connector.

1.3 Pin Assignment

EDC4000 uses a standard IDE pin-out. See Table 1 for EDC4000 pin assignments.

Table 1: EDC4000 Pin Assignment

Pin No.	Name	Function	Pin No.	Name	Function
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	40-pin VCC[1]	Supply Voltage
				44pin KEY[1]	Key-pin
21	DMARQ	DMA Request	22	GND	Ground
23	HIOW[3]	Host I/O Write	24	GND	Ground
	STOP[4]	Stop Ultra DMA burst			
25	HIOR[3]	Host I/O Read	26	GND	Ground
	HDMARDY[4]	Ultra DMA ready			
	HSTROBE[4]	Ultra DMA data strobe			
27	IORDY[3]	I/O Ready	28	CSEL	Master/Slave Select (Switch used)
	DDMARDY[4]	Ultra DMA ready			
	DSTROBE[4]	Ultra DMA data strobe			

29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
Pin No.	Name	Function	Pin No.	Name	Function
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2
37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41[2]	VCC	Supply Voltage	42[2]	VCC	Supply Voltage
43[2]	GND	Ground	44[2]	NC	Not Connected

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.
2. The 40-pin version does not contain pins 41-44.
   NC = These pins are not connected internally.
3. Signal usage in PIO & Multiword DMA mode.
4. Signal usage in Ultra DMA mode.

1.4 Pin Description

Table 2 describes the pin descriptions for EDC4000

Table 2: EDC4000 Pin Description

Pin Name	Pin No.	Description	I/O
Host side pins			
HRESET-	1	Host reset signal, High: Reset.	I
CS0-	37	Chip select CS0	I
CS1-	38	Chip select CS1	I
INTRQ	31	Host interrupt signal.	O
HIOR-[3]	25	I/O read strobe signal.	I
HDMARDY-[4]		DMA ready during Ultra DMA data in burst	
HSTROBE[4]		Data strobe during Ultra DMA data out burst	
HIOW-[3]	23	I/O write strobe signal.	I
STOP[4]		Stop during Ultra DMA data bursts	
IOCS16-	32	Asserted in 16-bit access.	O
IORDY[3]	27	I/O Ready Signal	O
DDMARDY-[4]		DMA ready during Ultra DMA data out burst	
DSTROBE[4]		Data strobe during Ultra DMA data in burst	
HDB[15:0]	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	Host data bus	I/O
HAB[2:0]	33, 35, 36	Host Address bus	I/O
CSEL-	28	Master/Slave select signal (cable select signal). Low: Device operates as a master, High: Device operates as a slave. Switch used.	I
DASP-	39	Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.	I/O
PDIAG-	34	Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.	I/O

DMARQ	21	DMA Request.	O
DMACK-	29	DMA Acknowledge.	I
Power and Ground			
VCC	20[1], 41[2], 42[2]	Connect to VCC	VCC
GND	2, 19, 22, 24, 26, 30, 40, 43[2]	Connect to GND.	GND
Other pins			
NC	44[2]	Not used. Please do not connect.	N/A

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.
2. The 40-pin version does not contain pins 41-44.
   NC = The pins are not connected internally.
3. Signal usage in PIO & Multiword DMA mode.
4. Signal usage in Ultra DMA mode.

2. Theory of operation

2.1 Overview

Figure 1 shows EDC4000 operation from the system level, including the major hardware blocks.

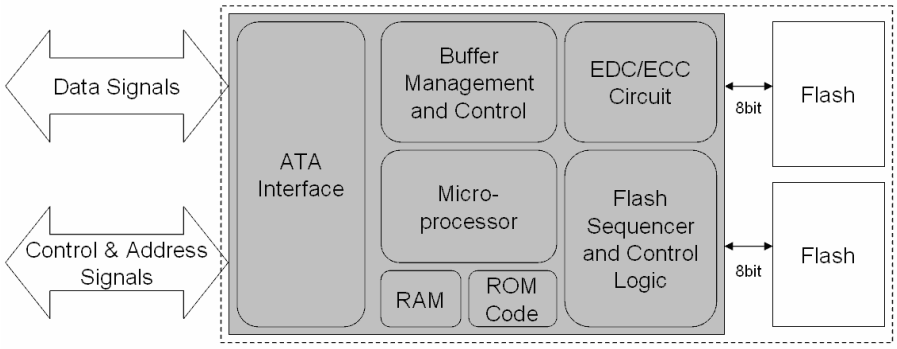


Figure 1: EDC4000 Block Diagram

EDC4000 integrates an IDE controller and flash devices. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

2.2 Controller

The controller is equipped with 16KB of internal memory that is used for storing code and data. The internal memory can also be used as an intermediate memory for storing data blocks during a wear-leveling procedure. An 8KB internal boot ROM includes basic routines for accessing the flash memories and for loading the main code into the internal memory.

2.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a algorithm that can correct four bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.4 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

EDC4000 uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

3. Installation Requirements

3.1 EDC4000 Pin Directions

Figure 2 and Figure 3 illustrate the EDC4000 pin directions.

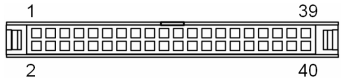


Figure 2: 40-pin Connector Layout (Female)

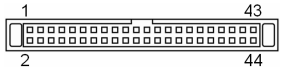


Figure 3: 44-pin Connector Layout (Female)

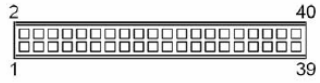


Figure 4: 40-pin Connect Layout (Male)

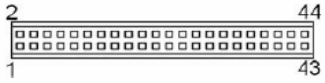


Figure 5: 44-pin Connector Layout (Male)

3.2 Electrical Connections for EDC4000

EDC4000 can be connected to the host by placing it directly on the on-board socket. If a cable is used, it should be no longer than 20 inches (457mm), and should be aligned as follows:

- For 40-pin EDC4000:

  Pin 1 of the cable must be aligned with pin 1 of the EDC4000 connector.

  Pin 40 of the cable must be aligned with pin 40 of the EDC4000 connector.

- For 44-pin EDC4000:

  Pin 1 of the cable must be aligned with pin 1 of the EDC4000 connector.

  Pin 44 of the cable must be aligned with pin 44 of the EDC4000 connector.

The 40-pin EDC4000 version has a separate connector for the power supply, to which a power supply cable can be connected. In addition, pin 20 can also be used for power supply connections. Please refer to the pin description for further details.

3.3 Installing EDC4000 in a Two-Drive Configuration (Master/Slave)

If EDC4000 is being installed as an additional IDE drive using the same IDE I/O port, Switch S1 in “M” position will be the master, whereas in “S” position it becomes the slave.

4. Power Management

EDC4000 supports the following two operation modes:

Sleep Mode: Internal clock is halted (for EDC4000, the standby mode defined in the ATA specification is the same as this mode)

Active Mode: Internal clock operates normally (for EDC4000, the idle mode defined in the ATA specification is the same as this mode)

5. Specifications

5.1 CE and FCC Compatibility

- **CE Compatibility**

EDC4000 conforms to CE requirements.

- **RoHS Compliance**

EDC4000 is fully compliant with RoHS directive.

5.2 Environmental Specifications

5.2.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: -10℃ to +70℃
- Industrial Grade: -40℃ to +85℃

Storage Temperature Range:

- Standard Grade: -55℃ to +95℃
- Industrial Grade: -55℃ to +95℃

5.2.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.2.3 Shock and Vibration

Table 3: Shock/Vibration Testing for EDC4000

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2 KHz, 5 g, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 10ms, 50 g, 3 axes	IEC 68-2-27
Drop Unit	From a height of 1.5 m	IEC 68-2-32

5.2.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various EDC4000 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.

- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 4: EDC4000 MTBF

Product	Condition	MTBF (Hours)
40-pin	Telcordia SR-332 GB, 25℃	> 3,000,000
44-pin		> 3,000,000

5.3 Mechanical Dimensions

40-pin

Mechanical Dimension: 60.2/6.4/27.79 mm (W/T/H)

Figure 6: Mechanical Dimension of EDC4000 40-pin

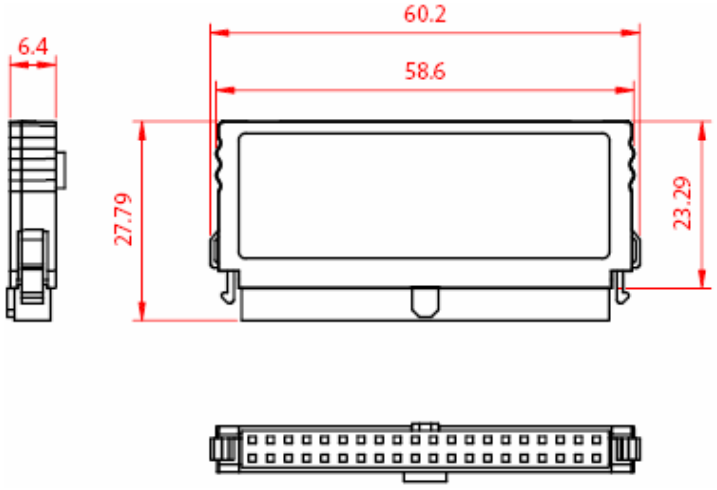


Figure 7: Mechanical Dimension of EDC4000 40-pin(Horizontal Female Type A)

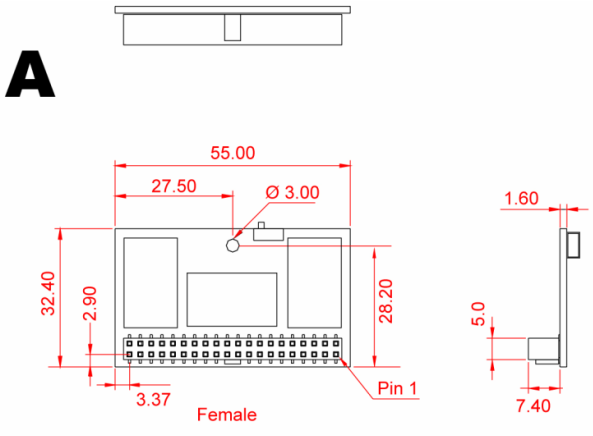


Figure 8: Mechanical Dimension of EDC4000 40-pin(Horizontal Female Type B)

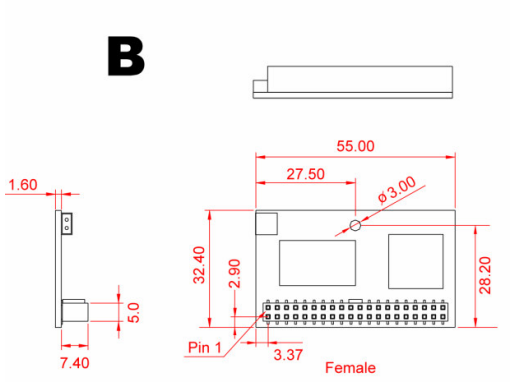


Figure 9: Mechanical Dimension of EDC4000 40-pin(Horizontal Male Type C)

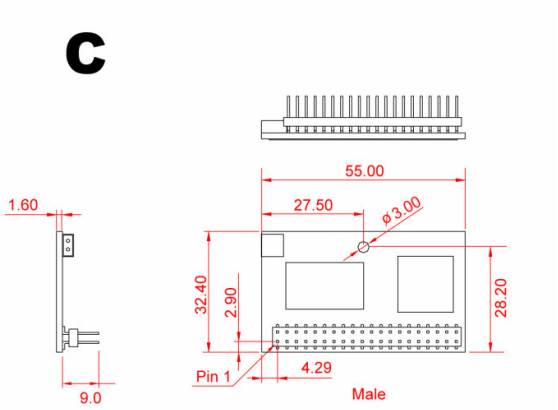


Figure 10: Mechanical Dimension of EDC4000 40-pin(Horizontal Male Type D)

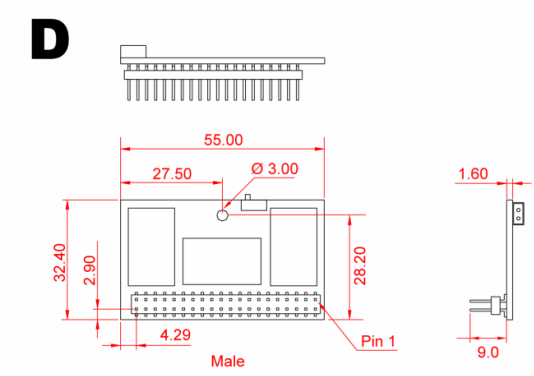


Figure 11: Mechanical Dimension of EDC4000 40-pin(Horizontal Female/Male Type E)

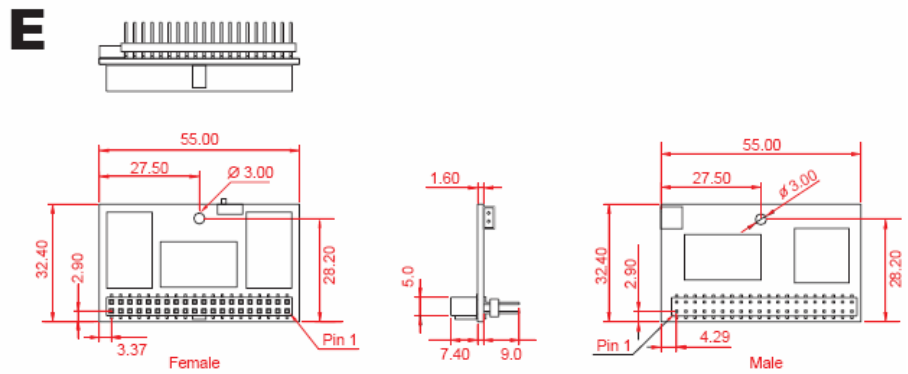
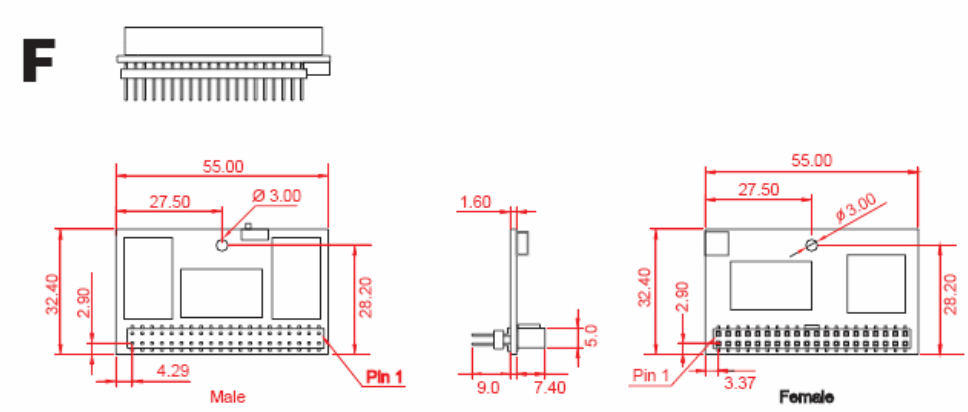


Figure 12: Mechanical Dimension of EDC4000 40-pin(Horizontal Male/Female Type F)



44-pin

Vertical Version Mechanical Dimension: 50.25/5.8/27.27 mm (W/T/H)

Horizontal Version Mechanical Dimension: 48.0/4.5/32.6 mm (W/T/H)

Figure 13: Mechanical Dimension of EDC4000 44-pin (Vertical Version)

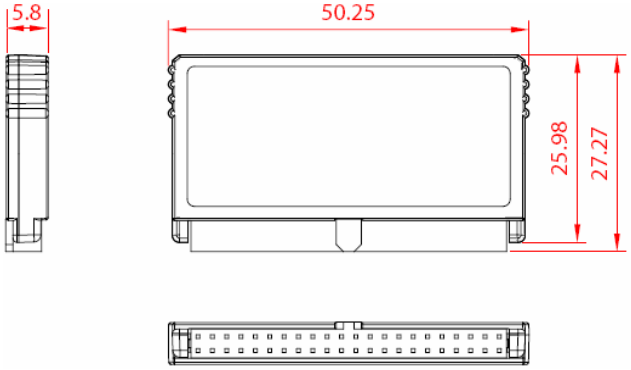


Figure 14: Mechanical Dimension of EDC4000 44-pin (Horizontal Female Type A)

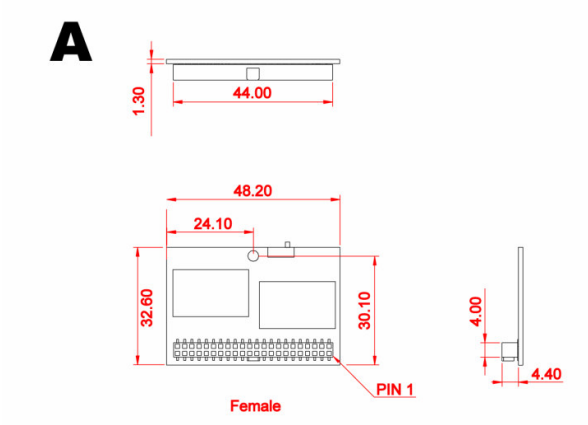


Figure 15: Mechanical Dimension of EDC4000 44-pin (Horizontal Female Type B)

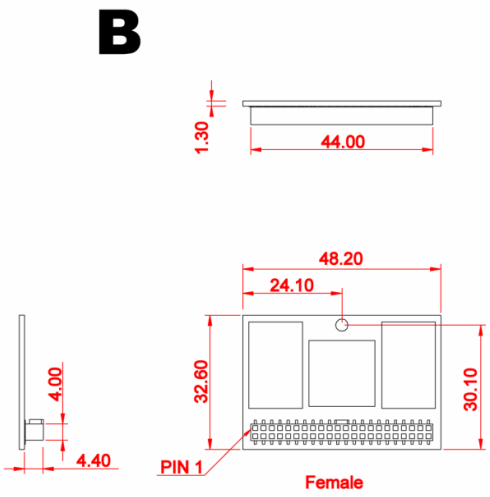


Figure 16: Mechanical Dimension of EDC4000 44-pin (Horizontal Male Type C)

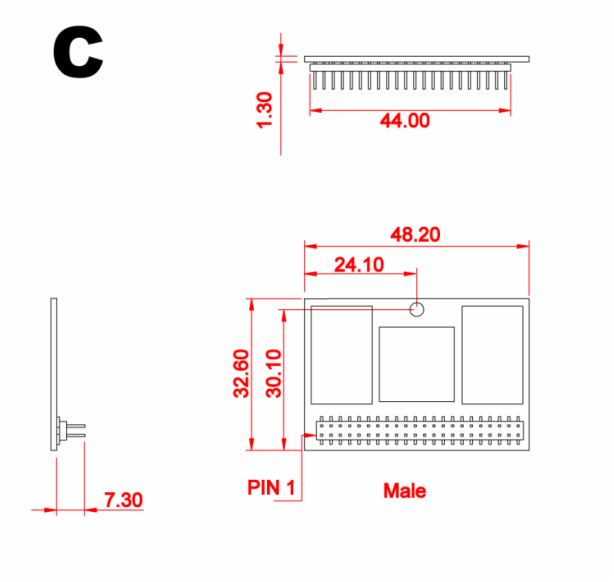


Figure 17: Mechanical Dimension of EDC4000 44-pin (Horizontal Male Type D)

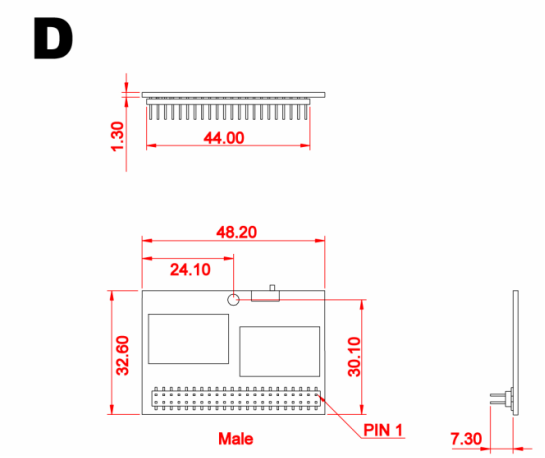


Figure 18: Mechanical Dimension of EDC4000 44-pin (Horizontal Female/Male Type E)

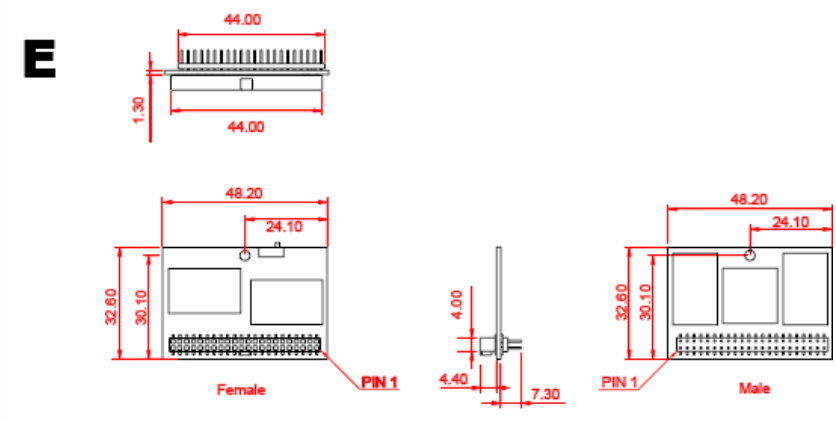
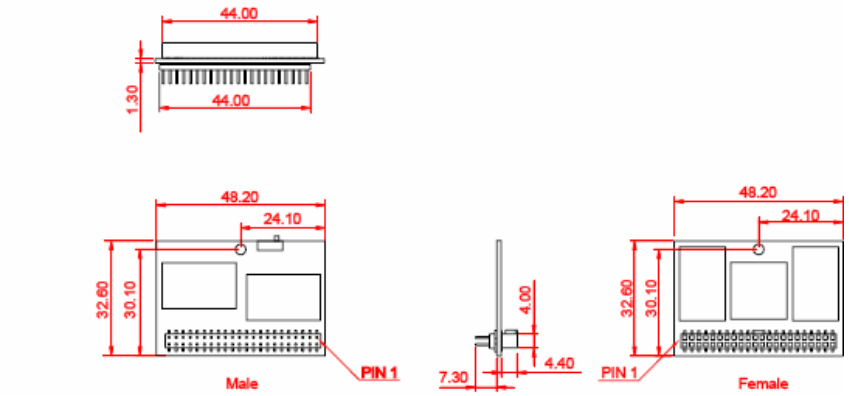


Figure 19: Mechanical Dimension of EDC4000 44-pin (Horizontal Male/Female Type F)

F



5.4 Electrical Specifications

5.4.1 Absolute Maximum Ratings

Table 5: EDC4000 Maximum Absolute Ratings

Item	Symbol	Rating	Unit
DC Power Supply	V_{DD} - V_{SS}	-0.3 ~ +5.5	V
Input voltage	V_{IN}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Output voltage	V_{OUT}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Operating Temperature	T_A	Standard: -10 ~ +70	℃
		Industrial: -40 ~ +85	℃
Storage Temperature	T_{ST}	Standard: -55 ~ +95	℃
		Industrial: -55 ~ +95	℃

Table 6: Schmitt Trigger Pin

Pin Name	IOL (mA)	Dir	
PinHOE, PinHWE, PinHIOR, PinHIOW	12	I	CMOS Level Pull-up 75K (SCHMITT)
Input voltage	12	I	CMOS Level Pull-up 75K (SCHMITT)
Output voltage	12	I	CMOS Level (SCHMITT)

5.4.2 DC Characteristic

Table 7: EDC4000 DC Characteristic

Item	Symbol	Value			Unit
		Min	Standard	Max	
Power Supply	VCCH	4.5	5.0	5.5	V
Power Supply	VCCF	3.0	3.3	3.6	V
Input low voltage	V_{IL}	-0.3		0.8	V

Input high voltage	V_{IH}	2.0		Vcc+0.3	V
Output low voltage	V_{OL}			0.45 (at 4mA)	V
Output high voltage	V_{OH}	2.4 (at 1mA)			V
Operating CurrentV Sleep Mode Operation	Icc			 1.4 140	 mA mA
Input Leakage Current	ILI			±10	uA
Output leakage current	L_{LO}			±10	μA
Input/output Capacitance	$C_{I/O}$			10	pF

5.5 Timing Specifications

- **PIO Mode**

Figure 20: Read/Write Timing Diagram, PIO Mode

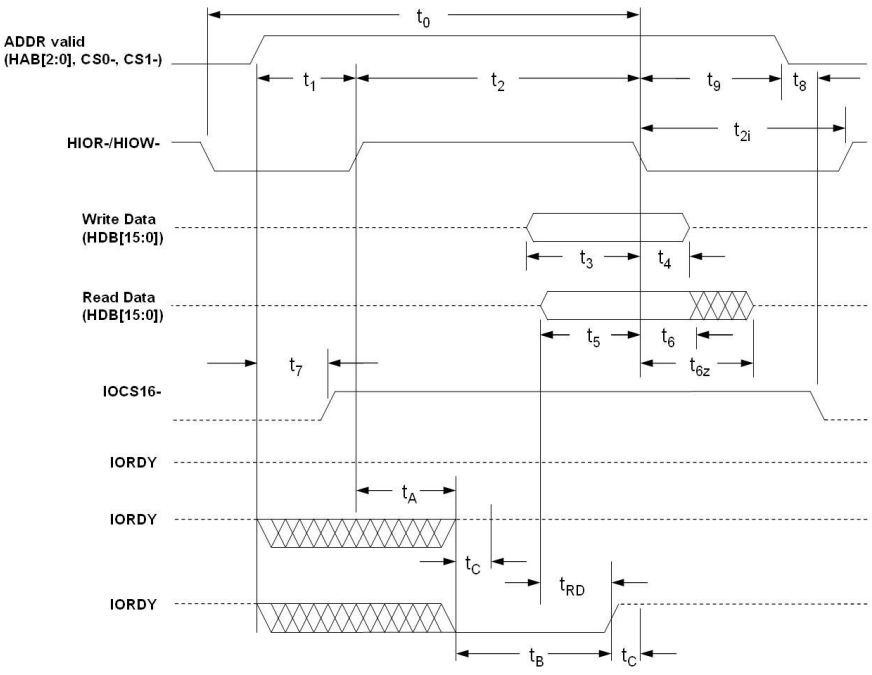


Table 8: Read/Write Timing Specifications, PIO Mode 0-4

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min.)	600	383	240	180	120
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70
t_2	HIOR-/HIOW- Register 8-bit (min.)	290	290	290	80	70
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25

t_3	HIOW- data setup (min.)	60	45	30	30	20
t_4	HIOW- data hold (min.)	30	20	15	10	10
t_5	HIOR- data setup (min.)	50	35	20	20	20
t_6	HIOR- data hold (min.)	5	5	5	5	5
t_{6Z}	HIOR- data tri-state (max.)	30	30	30	30	30
t_7	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a
t_8	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release (max.)	5	5	5	5	5

- **Multiword DMA**

Figure 21: Read/Write Timing Diagram, Multiword DMA Mode

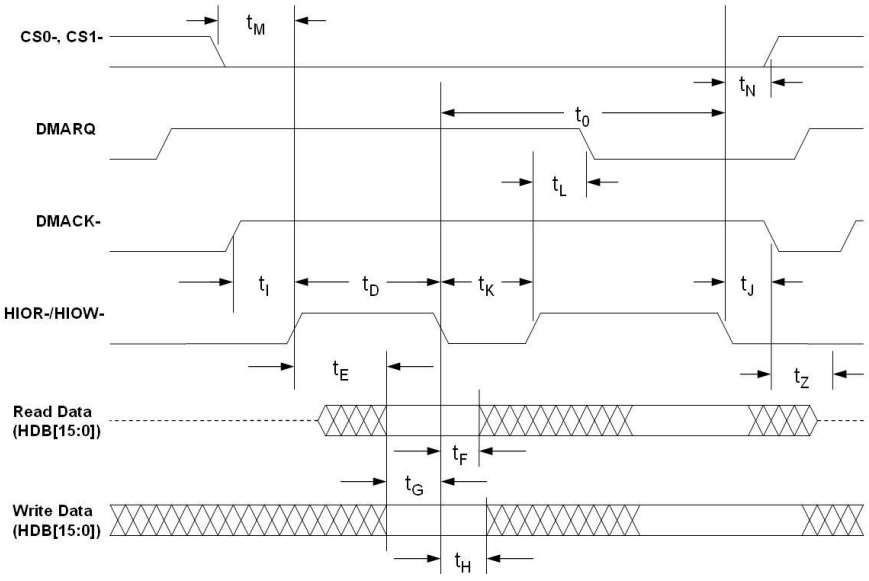


Table 9: Read/Write Timing Specifications, Multiword DMA Mode 0-2

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t_0	Cycle time (min.)	480	150	120
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70
t_E	HIOR- data access (max.)	150	60	50
t_F	HIOR- data hold (min.)	5	5	5
t_G	HIOR-/HIOW- data setup (min.)	100	30	20
t_H	HIOW- data hold (min.)	20	15	10
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5

t_{KR}	HIOR- negated width (min.)	50	50	25
t_{KW}	HIOW- negated width (min.)	215	50	25
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35
t_{M}	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25
t_{N}	CS1-, CS0- hold	15	10	10
t_{Z}	DMACK-	20	25	25

- **Ultra DMA mode**

Figure 22: Ultra DMA Mode Data-in Burst Initiation Timing Diagram

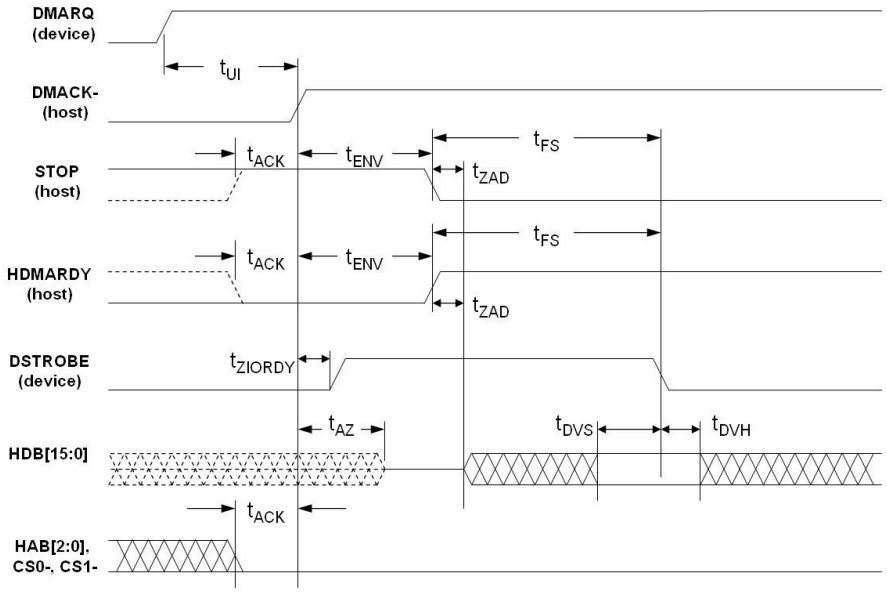


Figure 23: Ultra DMA Mode Data-out Burst Initiation Timing Diagram

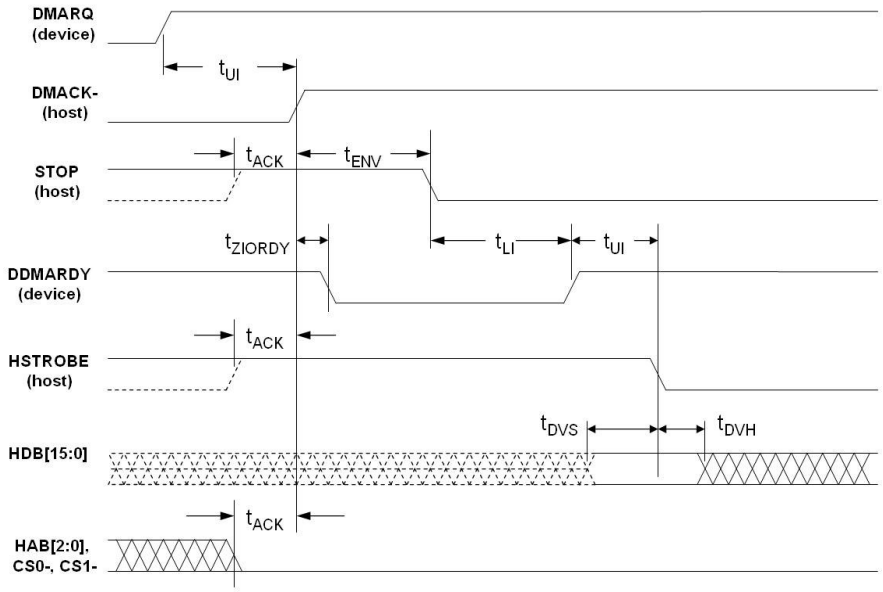


Figure 24: Sustained Ultra DMA Mode Data-in Burst Timing Diagram

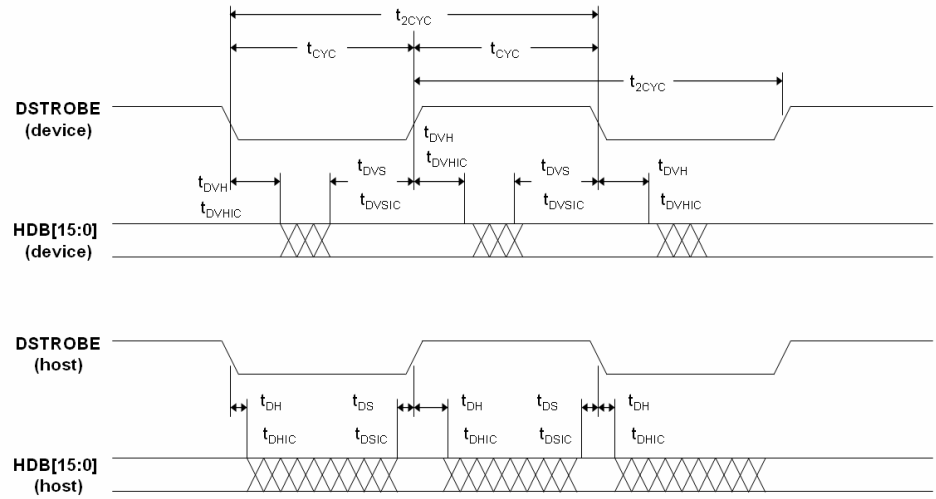


Figure 25: Sustained Ultra DMA Mode Data-out Burst Timing Diagram

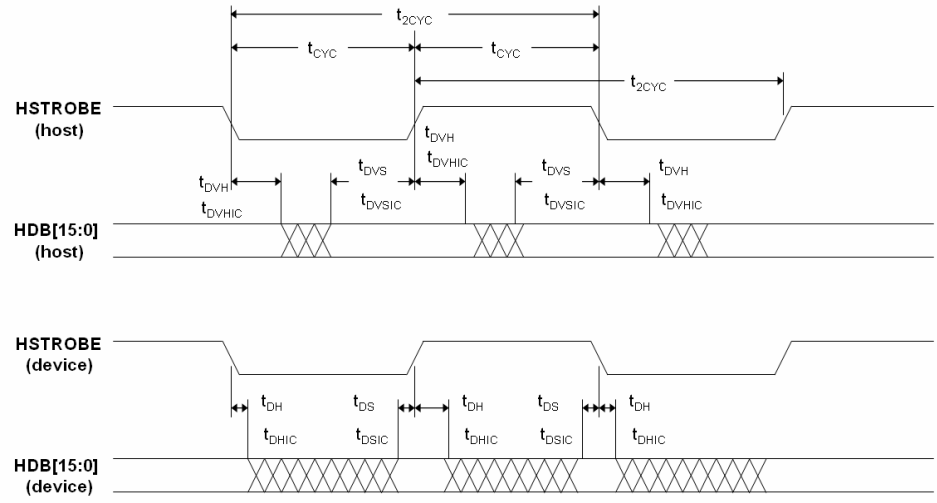


Table 10: Timing Diagram, Ultra DMA Mode 0-4

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	120	-	90	-	60	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	54	-	39	-	25	-
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	115	-	86	-	57	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	7	-	5	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	31	-	20	-	6.7	-
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	170	-	130	-	120
Ultra DMA timing parameters		**Mode 0**		**Mode 1**		**Mode 2**		**Mode 3**		**Mode 4**	
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
t_{LI}	Limited interlock time	0	150	0	150	0	150	0	100	0	100
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	20	-	20	-	20	-	20	-
t_{ZAD}		0	-	0	-	0	-	0	-	0	-
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	70	20	55	20	55
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60

t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	20	-	20	-

6. Supported IDE Commands

EDC4000 supports the commands listed in Table 11.

Table 11: IDE Commands

Command Name	Command Code
Check Power Mode	98H or E5H
Execute Device Diagnostic	90H
Erase Sector	C0H
Format Track	50H
Identify Device	ECH
Idle	97H or E3H
Idle immediate	95H or E1H
Initialize Device Parameters	91H
NOP	00H
Read Buffer	E4H
Read Long Sector	22H or 23H
Read Multiple	C4H
Read Sector	20H or 21H
Read Verify Sector	40H or 41H
Recalibrate	1XH
Seek	7XH
Set Features	EFH
Set Multiple Mode	C6H
Set Sleep Mode	99H or E6H
Standby	96H or E2H
Standby Immediate	94H or E0H
Write Buffer	E8H
Write Long Sector	32H or 33 H
Write Multiple	C5H
Write Sector	30H or 31H
Write Verify	3CH

7. Device Parameters

EDC4000 device parameters listed in Table 12.

Table 12: Device parameters

Capacity	Total number of sectors	Cylinders	Heads	Sectors
32MB	64000	500	8	16
64MB	128000	500	8	32
128MB	256000	500	16	32
256MB	512000	1000	16	32
512MB	1023120	1015	16	63
1GB	2047248	2031	16	63
2GB	4095504	4063	16	63
4GB	8211168	8146	16	63
8GB	16128000	16000	16	63