InnoDisk iCF4000

Industrial CompactFlash® Card 4000

Datasheet

Ver 1.3

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REVISION HISTORY

Revision	Description	Date
1.0	Release First Version	December 2007
1.1	Add Reset Timing	March 2008
1.2	Add Power Consumption Table	March 2008
1.3	Modify Storage Temperature & release 8GB availability	April 2008

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1. Introduction

The InnoDisk Industrial CompactFlash® 4000 Memory Card (iCF4000) products provide high capacity solid-state flash memory that electrically complies with the Personal Computer Memory Card International Association (PCMCIA) ATA (PC Card ATA) standard. (In Japan, the applicable standards group is JEIDA.) The CompactFlash® and PCMCIA cards support True IDE Mode that is electrically compatible with an IDE disk drive. The original CF form factor card can be used in any system that has a CF slot. Designed to replace traditional rotating disk drives, InnoDisk Industrial CompactFlash® 4000 Memory Cards are embedded solid-state data storage systems for mobile computing and the industrial work place. These Industrial CompactFlash® feature an extremely lightweight, reliable, low-profile form factor.

Industrial CompactFlash® 4000 (iCF4000) supports advanced PIO (0-6), Multiword DMA (0-4), Ultra DMA (0-4) transfer modes, multi-sector transfers, and LBA addressing.

2. Features

The Industrial ATA products provide the following system features:

- Capacities: 32MB, 64MB, 128MB, 256MB, 512MB, 1GB, 2GB, 4GB and 8GB
- Fully compatible with CompactFlash® specification version 3.0
- Fully compatible with PC Card Standard.
- Fully compatible with the IDE standard interface, ATA Standard
- Three access modes
  - PC Card Memory Mode
  - PC Card I/O Mode
  - True IDE Mode
- High reliability based on the internal ECC (Error Correction Code) function
- +3.3V/+5V single power supply operation
- Support Auto Stand-by and Sleep Mode.

- Power consumption

Single

◆ 5V

Active mode

Read operation: 69mA (Typ.)

Write operation: 59mA (Typ.)

Power down mode: 1.2mA (Typ./max.)

◆ 3.3V

Active mode

Read operation: 67mA (Typ.)

Write operation: 52mA (Typ.)

Power down mode: 0.7mA (Typ./max.)

Dual

◆ 5V

Active mode

Read operation: 125mA (Typ.)

Write operation: 120mA (Typ.)

Power down mode: 1.3 (Typ./max.)

◆ 3.3V

Active mode

Read operation: 121mA (Typ.)

Write operation: 115mA (Typ.)

Power down mode: 0.6mA (Typ.) 0.7(max.)

- Support transfer modes: PIO(0-6), Multiword DMA (0-4) and Ultra DMA(0-4)
- MTBF > 3,000,000 hours
- Minimum 10,000 insertions
- Endurance: 2,000,000 Program/Erase Cycles
- R/W performance:
  - 32MB, 64MB, 128MB, 256MB, 512MB, 1GB, 2GB: Single Channel Mode
    - ◆ Read: 20MBytes/s. (MAX)
    - ◆ Write: 8MBytes/s (MAX)

- 1GB, 2GB, 4GB, 8GB: Dual Channel Mode
  - Read: 40Mbytes/s. (MAX)
  - Write: 20Mbytes/s (MAX)

- Operating temperature range:
  - Standard Grade: -10℃ ~ +70℃
  - Industrial Grade: -40℃ ~ +85℃
- Storage temperature range:
  - Standard Grade: -55℃ ~ +95℃
  - Industrial Grade: -55℃ ~ +95℃

3. Pin Assignment

See Table 1 for iCF4000 pin assignments.

Table 1: iCF4000 Pin Assignments

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	Name	I/O	Pin No.	Name	I/O	Pin No.	Name	I/O
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10[2]	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09[2]	I
11	A08	I	11	A08	I	11	A08[2]	I
12	A07	I	12	A07	I	12	A07[2]	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06[2]	I
15	A05	I	15	A05	I	15	A05[2]	I
16	A04	I	16	A04	I	16	A04[2]	I
17	A03	I	17	A03	I	17	A03[2]	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOCS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O
27	D11[1]	I/O	27	D11[1]	I/O	27	D11[1]	I/O
28	D12[1]	I/O	28	D12[1]	I/O	28	D12[1]	I/O
29	D13[1]	I/O	29	D13[1]	I/O	29	D13[1]	I/O
30	D14[1]	I/O	30	D14[1]	I/O	30	D14[1]	I/O
31	D15[1]	I/O	31	D15[1]	I/O	31	D15[1]	I/O
32	-CE2[1]	I	32	-CE2[1]	I	32	-CS1[1]	I

33	-VS1	O	33	-VS1	O	33	-VS1	O
34	-IORD	I	34	-IORD	I	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I
35	-IOWR	I	35	-IOWR	I	35	-IOWR[7] STOP[8, 9]	I
36	-WE	I	36	-WE	I	36	-WE[3]	I
37	READY	O	37	-IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	-CSEL[5]	I	39	-CSEL[5]	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	O
41	RESET	I	41	RESET	I	41	-RESET	I
42	-WAIT	O	42	-WAIT	O	42	IORDY[1] -DDMARDY[8] DSTROBE[9]	O
43	-INPACK	O	43	-INPACK	O	43	DMARQ	O
44	-REG	I	44	-REG	I	44	-DMACK[6]	I
45	BVD2	O	45	-SPKR	O	45	-DASP	I/O
46	BVD1	O	46	-STSCHG	O	46	-PDIAG	I/O
47	D08[1]	I/O	47	D08[1]	I/O	47	D08[1]	I/O
48	D09[1]	I/O	48	D09[1]	I/O	48	D09[1]	I/O
49	D10[1]	I/O	49	D10[1]	I/O	49	D10[1]	I/O
50	GND		50	GND		50	GND	

Note:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
2) The signal should be grounded by the host.
3) The signal should be tied to VCC by the host.
4) The mode is optional for CF+ Cards, but required for CompactFlash® Storage Cards.
5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition
7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

4. Pin Description

Table 2 describes the pin descriptions for iCF4000

Table 2: iCF4000 Pin Description

Pin No.	Pin Name	I/O	Mode	Description
8,10,11, 12,14, 15,16, 17,18, 19, 20	A10 – A0	I	PC Card Memory Mode	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash® Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash® Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
8,10,11, 12,14, 15,16, 17,18, 19, 20	A10 – A0		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
18,19, 20	A2 – A0		True IDE Mode	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
46	BVD1	I/O	PC Card Memory Mode	This signal is asserted high, as BVD1 is not supported.
	-STSCHG		PC Card I/O Mode	This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card configuration and Status Register.
	-PDIAG		True IDE Mode	In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
45	BVD2	I/O	PC Card Memory Mode	This signal is asserted high, as BVD2 is not supported.
	-SPKR		PC Card I/O Mode	This line is the Binary Audio output from the card. If the Card does not support the Binary

				Audio function, this line should be held negated.
	-DASP		True IDE Mode	In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
26, 25	-CD1, -CD2	O	PC Card Memory Mode	These Card Detect pins are connected to ground on the CompactFlash® Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash® Storage Card or CF+ Card is fully inserted into its socket.
			PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
7, 32	-CE1, -CE2	I	PC Card Memory Mode	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.
	-CE1, -CE2		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	-CS0, -CS1		True IDE Mode	In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
39	-CSEL	I	PC Card Memory Mode	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
			PC Card I/O Mode	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
			True IDE Mode	This internally pulled up signal is used to configure this device as a Master or a Slave

				when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
2,3,4,5, 6,31,30 29,28, 27,49, 48,47, 23,22, 21	D15 - D00	I/O	PC Card Memory Mode	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
			PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
			True IDE Mode	In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
1, 50	GND	-	PC Card Memory Mode	Ground.
			PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
43	-INPACK	O	PC Card Memory Mode	This signal is not used in this mode.
	-INPACK		PC Card I/O Mode	The Input Acknowledge signal is asserted by the CompactFlash® Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash® Storage Card or CF+ Card and the CPU.
	DMARQ		True IDE Mode	This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK, i.e., the device shall wait until the

				host asserts -DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
34	-IORD	I	PC Card Memory Mode	This signal is not used in this mode.
			PC Card I/O Mode	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash® Storage Card or CF+ Card when the card is configured to use the I/O interface.
	-IORD		True IDE Mode	In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
	-HDMARDY			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate -HDMARDY to pause an Ultra DMA transfer.
	HSTROBE			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra

				DMA data-out burst.
35	-IOWR	I	PC Card Memory Mode	This signal is not used in this mode.
	-IOWR		PC Card I/O Mode	The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash® Storage Card or CF+ Card controller registers when the CompactFlash® Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
	-IOWR		True IDE Mode	In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
	STOP			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
9	-OE	I	PC Card Memory Mode	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash® Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
	-OE		PC Card I/O Mode	In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
	-ATA SEL		True IDE Mode	To enable True IDE Mode this input should be grounded by the host.
37	READY	O	PC Card Memory Mode	In Memory Mode, this signal is set high when the CompactFlash® Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash® Storage Card or CF+ Card has

				completed its power up or reset function. No access of any type should be made to the CompactFlash® Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
	-IREQ		PC Card I/O Mode	I/O Operation – After the CompactFlash® Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
	INTRQ		True IDE Mode	In True IDE Mode signal is the active high Interrupt Request to the host.
44	-REG	I	PC Card Memory Mode	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
			PC Card I/O Mode	The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
	-DMACK		True IDE Mode	This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
41	RESET	I	PC Card	The CompactFlash® Storage Card or CF+ Card

			Memory Mode	is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash® Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
	RESET		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	-RESET		True IDE Mode	In the True IDE Mode, this input pin is the active low hardware reset from the host.
13, 38	VCC	-	PC Card Memory Mode	+5 V, +3.3 V power.
			PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
33, 40	-VS1, -VS2	O	PC Card Memory Mode	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash® Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
			PC Card I/O Mode	This signal is the same for all modes.
			True IDE Mode	This signal is the same for all modes.
42	-WAIT	O	PC Card Memory Mode	The -WAIT signal is driven low by the CompactFlash® Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
	-WAIT		PC Card I/O Mode	This signal is the same as the PC Card Memory Mode signal.
	IORDY		True IDE Mode	In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.

	-DDMARDY			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer.
	DSTROBE			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
36	-WE	I	PC Card Memory Mode	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash® Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
			PC Card I/O Mode	In PC Card I/O Mode, this signal is used for writing the configuration registers.
			True IDE Mode	In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
24	WP	O	PC Card Memory Mode	Memory Mode – The CompactFlash® Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
	-IOIS16		PC Card I/O Mode	I/O Operation – When the CompactFlash® Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
	-IOCS16		True IDE Mode	In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

5. Specifications

5.1 CE Compatibility

iCF4000 conforms to CE requirements.

5.2 RoHS Compliance

iCF4000 is fully compliant with RoHS directive.

5.3 Environmental Specifications

5.3.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: -10℃ to +70℃
- Industrial Grade: -40℃ to +85℃

Storage Temperature Range:

- Standard Grade: -55℃ to +95℃
- Industrial Grade: -55℃ to +95℃

5.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.3.3 Shock and Vibration

Table 3: Shock/Vibration Test for iCF4000

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2` KHz, 5 g, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 10ms, 50 g, 3 axes	IEC 68-2-27
Drop Unit	From a height of 1.5 m	IEC 68-2-32

5.3.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various iCF4000 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval

under stated conditions.

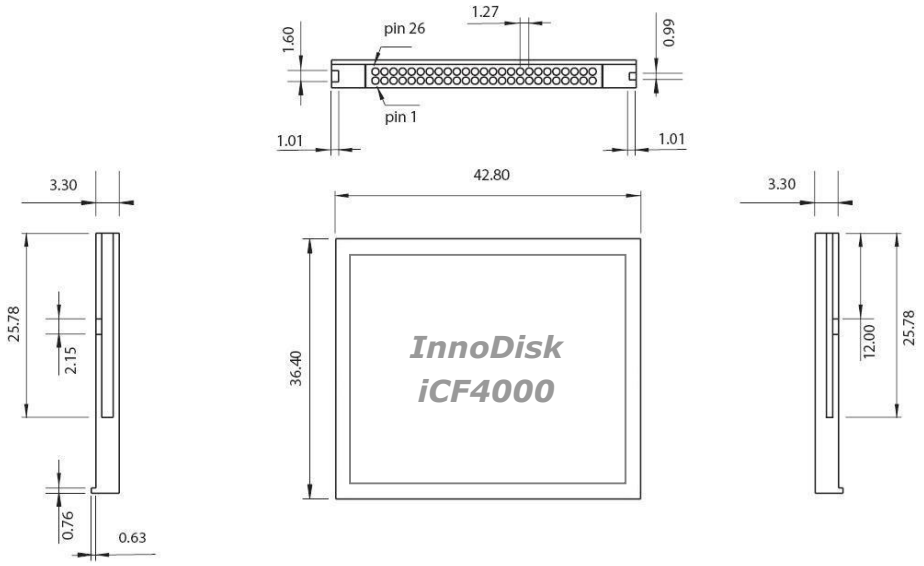
Table 4: iCF40000 MTBF

Product	Condition	MTBF (Hours)
iCF4000	Telcordia SR-332 GB, 25℃	> 3,000,000

5.4 Mechanical Dimensions

Mechanical Dimension: 42.80/36.40/3.30mm (W/T/H)

Figure 1: Mechanical Dimension of iCF4000



5.5 Electrical Specifications

5.5.1 Absolute Maximum Ratings

Table 5: iCF4000 Maximum Absolute Ratings

Item	Symbol	Rating	Unit
DC Power Supply	V_{DD} - V_{SS}	-0.3 ~ +5.5	V
Input voltage	V_{IN}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Output voltage	V_{OUT}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Operating Temperature	T_A	Commercial: -10 ~ +70	℃
		Industrial: -40 ~ +85	℃
Storage Temperature	T_{ST}	Commercial: -55 ~ +95	℃
		Industrial: -55 ~ +95	℃

Table 6: Schmitt Trigger Pin

Pin Name	IOL (mA)	Dir	
PinHOE, PinHWE, PinHIOR, PinHIOW	12	I	CMOS Level Pull-up 75K (SCHMITT)
Input voltage	12	I	CMOS Level Pull-up 75K (SCHMITT)
Output voltage	12	I	CMOS Level (SCHMITT)

5.5.2 DC Characteristic

Table 7: iCF4000 DC Characteristic

Item	Symbol	Value			Unit
		Min	Standard	Max	
Power Supply	VCCH	4.5	5.0	5.5	V
Power Supply	VCCF	3.0	3.3	3.6	V
Input low voltage	V_{IL}	-0.3		0.8	V
Input high voltage	V_{IH}	2.0		Vcc+0.3	V
Output low voltage	V_{OL}			0.45 (at 4mA)	V
Output high voltage	V_{OH}	2.4 (at 1mA)			V
Operating CurrentV Sleep Mode Operation	Icc			 1.4 140	 mA mA

Input Leakage Current	ILI			±10	uA
Output leakage current	L_{LO}			±10	µA
Input/output Capacitance	$C_{I/O}$			10	pF

5.5.3 Timing Specifications

5.5.3.1 Attribute Memory Read Timing Specification

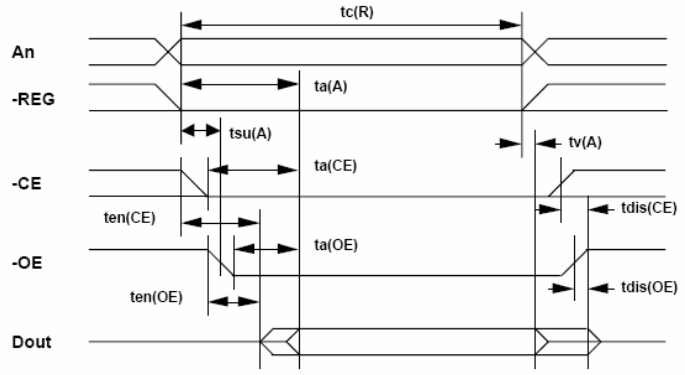
Attribute Memory access time is defined as 300ns. Detailed timing specs are shown in Table 8.

Table 8: Attribute Memory Read Timing

Speed Version			**300ns**	
Item	**Symbol**	**IEEE Symbol**	**Min (ns)**	**Max (ns)**
Read cycle time	tc(R)	tAVAV	300	
Address access time	ta(A)	tAVQV		300
Card enable access time	ta(CE)	tELQV		300
Output enable access time	ta(OE)	tGLQV		150
Output disable time from CE	tdis(CE)	tEHQZ		100
Output disable time from OE	tdis(OE)	tGHQZ		100
Address setup time	tsu(A)	tAVGL	30	
Output enable time from CE	ten(CE)	tELQNZ	5	
Output enable time from OE	ten(OE)	tGLQNZ	5	
Data valid from address change	tv(A)	tAXQX	0	

Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.

Figure 2: Attribute Memory Read Timing Diagram



5.5.3.2 Configuration Register (Attribute Memory) Write Timing Specification

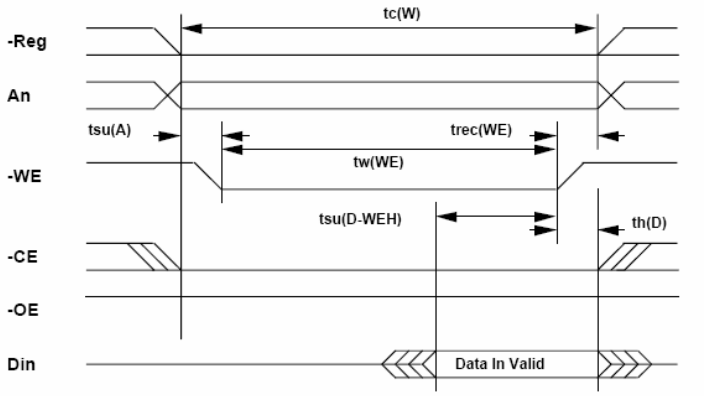
The Card Configuration write access time is defined as 250ns. Defined timing specifications are shown in Table 9.

Table 9: Configuration Register (Attribute Memory) Write Timing

Speed Version			250ns	
Item	**Symbol**	**IEEE Symbol**	**Min (ns)**	**Max (ns)**
Write cycle time	tc(W)	tAVAV	250	
Write pulse width	tw(WE)	tWLWH	150	
Address setup time	tsu(A)	tAVWL	30	
Write recovery time	trec(WE)	tWMAX	30	
Data setup time for WE	tsu(D-WEH)	tDVWH	80	
Data hold time	th(D)	tWMDX	30	

Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash storage card or CF+ card.

Figure 3: Configuration Register (Attribute Memory) Write Timing Diagram



5.5.3.3 Common Memory Read Timing Specification

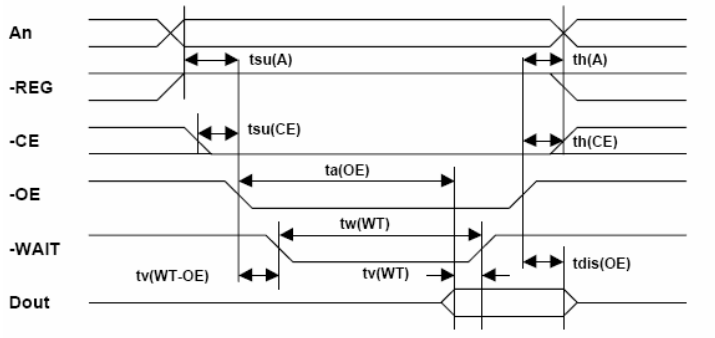
Table 10: Common Memory Read Timing

Cycle Time Mode:			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output enable access time	ta(OE)	tGLQV		125		60		50		40
Output disable time from OE	tdis(OE)	tGHQZ		100		60		50		40
Address setup time	tsu(A)	tAVGL	30		15		10		10	
Address hold time	th(A)	tGHAX	20		15		15		10	
CE setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait delay falling from OE	tv(WT-OE)	tGLWTV		35		35		35		Na
Data setup for wait release	tv(WT)	tQVWTH		0		0		0		Na
Wait width time	tw(WT)	tWTLWTH		350 (3000 for CF+)		350 (3000 for CF+)		350 (3000 for CF+)		Na

Note: 1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

Figure 4: Common Memory Read Timing Diagram



5.5.3.4 Common Memory Write Timing Specification

Table 11: Common Memory Write Timing

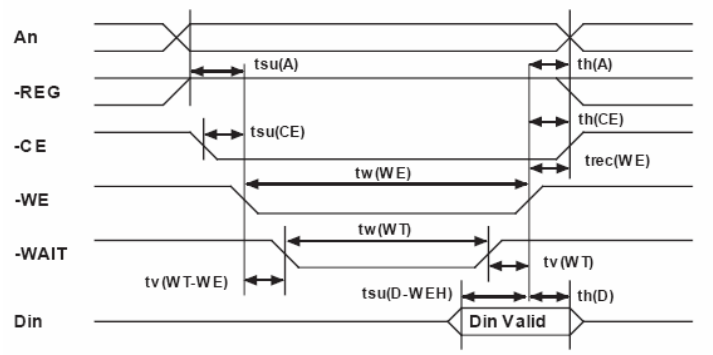
Cycle Time Mode:			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	

CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35		35		35		Na
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na	
Wait Width Time	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		Na

Notes: 1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12μs but is intentionally less in this specification.

Figure 5: Common Memory Write Timing Diagram



5.5.3.5 I/O Input (Read) Timing Specification

Table 12: I/O Read Timing

Cycle Time Mode:			250ns		120ns		100ns		80ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before	tsuCE(IORD)	tELIGL	5		5		5		5	

IORD										
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45	0	Na1	0	Na1	0	Na1
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45		Na1		Na1		Na1
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35		Na1		Na1		Na1
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35		Na1		Na1		Na1
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL		35		35		35		Na2
Data Delay from	td(WT)	tWTHQV		0		0		0		Na2

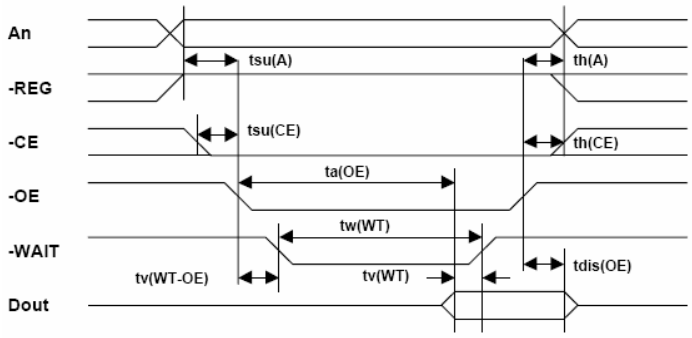
Wait Rising										
Wait Width Time	tw(WT)	tWTLWTH		350 (3000 for CF+)		350 (3000 for CF+)		350 (3000 for CF+)		Na2

Notes:1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.

Figure 6: I/O Read Timing Diagram



5.5.3.6 I/O Input (Write) Timing Specification

Table 13: I/O Write Timing

Cycle Time Mode:			250ns		120ns		100ns		80ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		25	

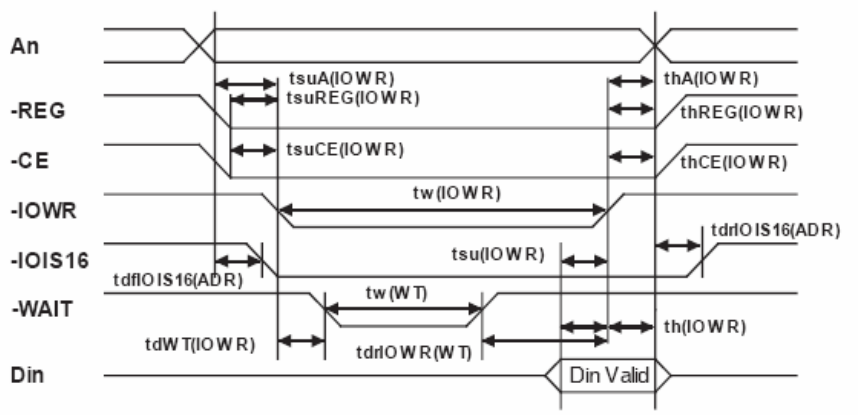
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35		Na1		Na1		Na1
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35		Na1		Na1		Na1
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL		35		35		Na2		Na2
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0		0			0		Na2
Wait Width Time	tw(WT)	tWTLWTH		350 (3000 for CF+)		350 (3000 for CF+)		350 (3000 for CF+)		Na2

Notes: 1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.

Figure 7: I/O Write Timing Diagram



5.5.3.7 True IDE PIO Mode Read/Write Timing Specification

Figure 8: Read/Write Timing Diagram, PIO Mode

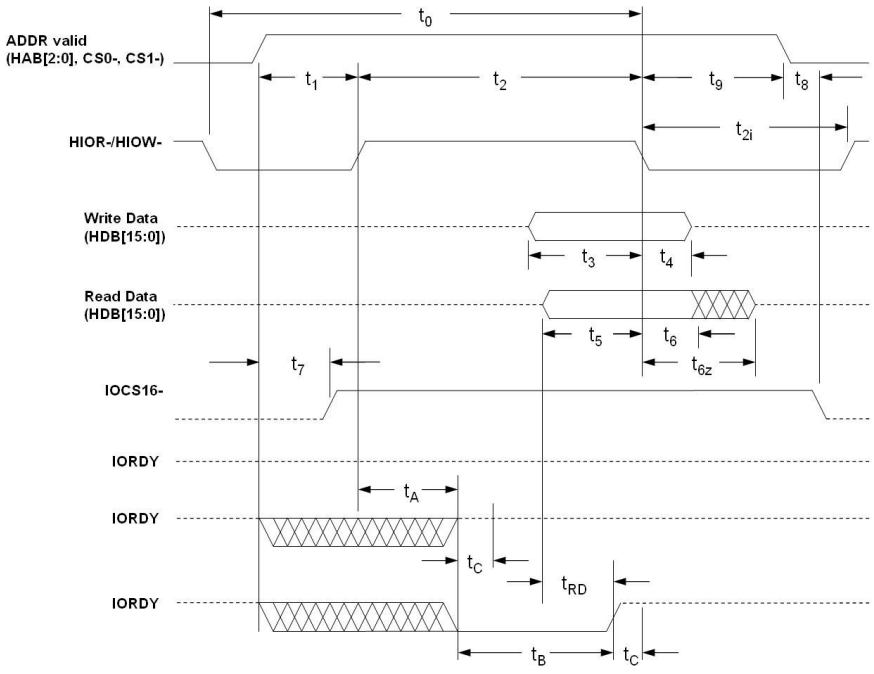


Table 14: Read/Write Timing Specifications, PIO Mode 0-6

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t_0	Cycle time (min.)	600	383	240	180	120	100	80
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25	15	10
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70	65	55
t_2	HIOR-/HIOW- Register 8-bit (min.)	290	290	290	80	70	65	55
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25	25	20
t_3	HIOW- data setup (min.)	60	45	30	30	20	20	15
t_4	HIOW- data hold (min.)	30	20	15	10	10	5	5
t_5	HIOR- data setup (min.)	50	35	20	20	20	15	10
t_6	HIOR- data hold (min.)	5	5	5	5	5	5	5
t_{6z}	HIOR- data tri-state (max.)	30	30	30	30	30	20	20
t_7	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a	n/a	n/a
t_8	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a	n/a	n/a
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35	n/a	n/a
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250	n/a	n/a
t_C	IORDY assertion to release (max.)	5	5	5	5	5	n/a	n/a

5.5.3.8 True IDE Multiword DMA Mode Read/Write Timing Specification

Figure 9: Read/Write Timing Diagram, Multiword DMA Mode

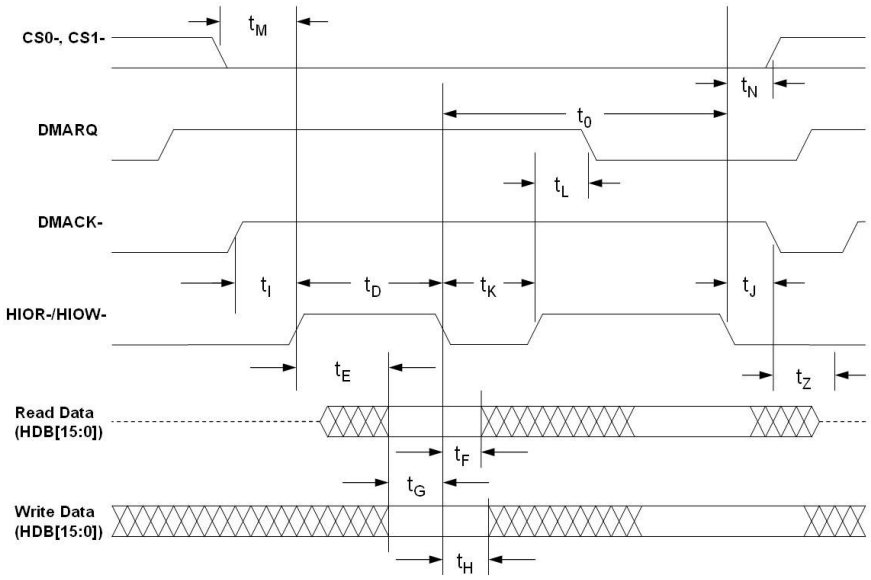


Table 15: Read/Write Timing Specifications, Multiword DMA Mode 0-4

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min.)	480	150	120	100	80
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70	65	55
t_E	HIOR- data access (max.)	150	60	50	50	45
t_F	HIOR- data hold (min.)	5	5	5	5	5
t_G	HIOR-/HIOW- data setup (min.)	100	30	20	15	10
t_H	HIOW- data hold (min.)	20	15	10	5	5
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5	5	5
t_{KR}	HIOR- negated width (min.)	50	50	25	25	20
t_{KW}	HIOW- negated width (min.)	215	50	25	25	20
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35	35	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35	35	35
t_M	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25	10	5
t_N	CS1-, CS0- hold	15	10	10	10	10
t_Z	DMACK-	20	25	25	25	25

5.5.3.9 True IDE Ultra DMA Mode Read/Write Timing Specification

Figure 10: Ultra DMA Mode Data-in Burst Initiation Timing Diagram

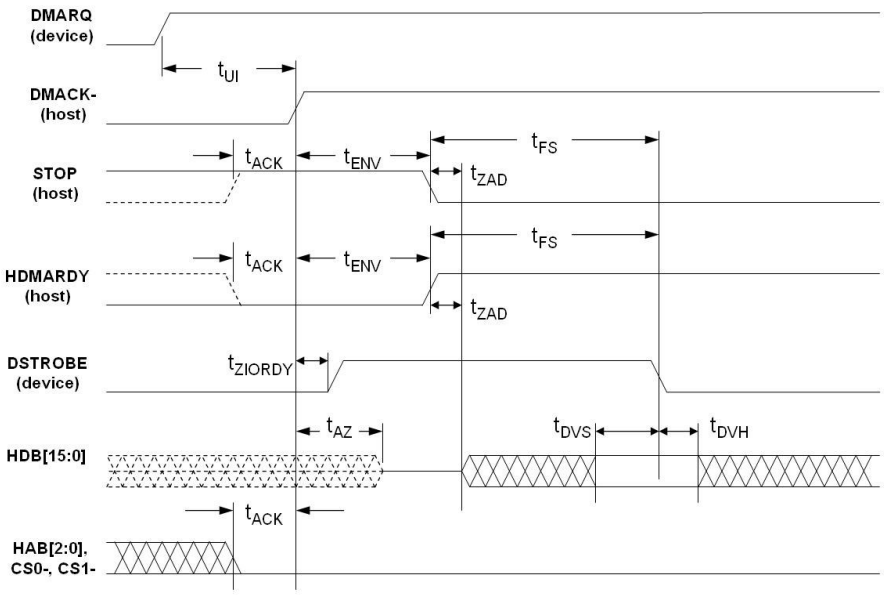


Figure 11: Ultra DMA Mode Data-out Burst Initiation Timing Diagram

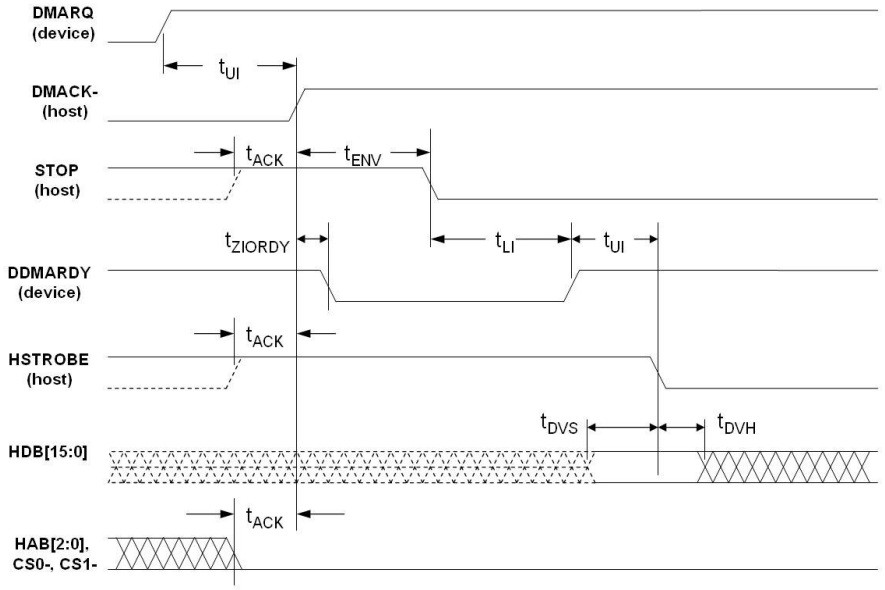


Figure 12: Sustained Ultra DMA Mode Data-in Burst Timing Diagram

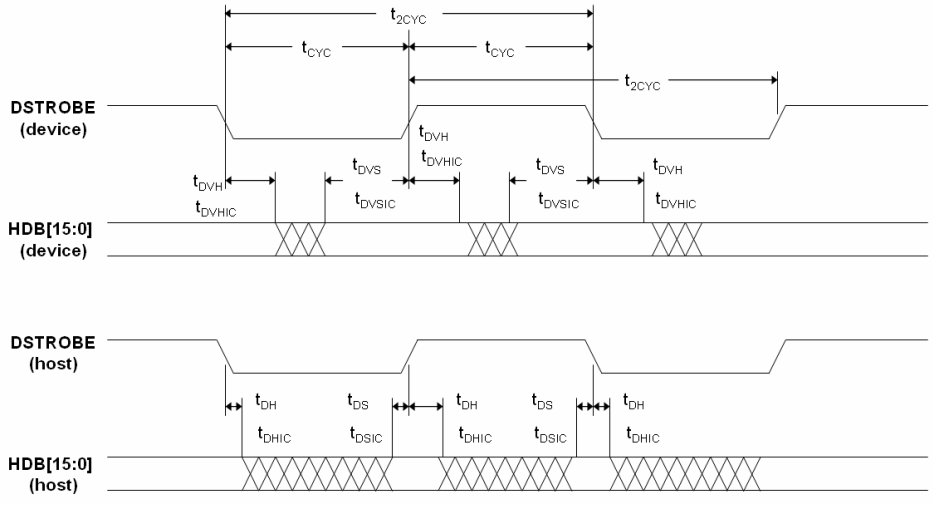


Figure 13: Sustained Ultra DMA Mode Data-out Burst Timing Diagram

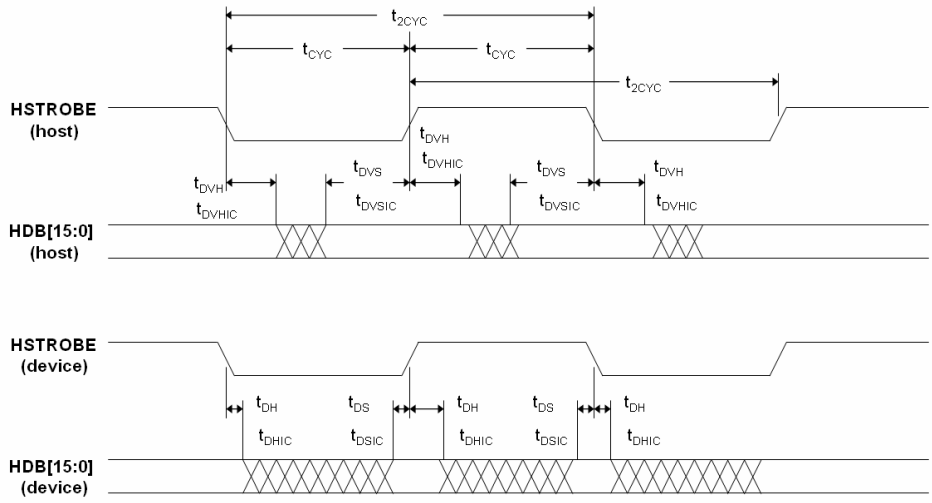


Table 16: Timing Diagram, Ultra DMA Mode 0-4

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	120	-	90	-	60	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	54	-	39	-	25	-
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	115	-	86	-	57	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	7	-	5	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	31	-	20	-	6.7	-
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	170	-	130	-	120

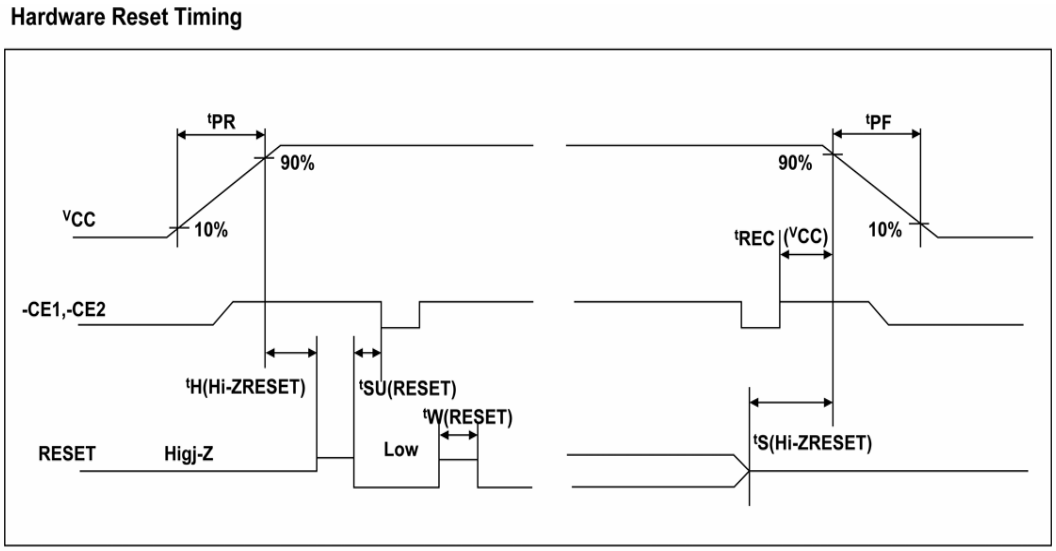
Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{LI}	Limited interlock time	0	150	0	150	0	150	0	100	0	100
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	20	-	20	-	20	-	20	-
t_{ZAD}		0	-	0	-	0	-	0	-	0	-
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	70	20	55	20	55
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	20	-	20	-

5.6 Hardware Reset(Only for Memory Card mode and I/O Card Mode)

Table 17: Timing Diagram, Hardware Reset

	Item	Min.	Max.	Normal	Unit
t_{SU}(RESET)	Reset Setup Time	20	-	-	ms
t_{REC}(VCC)	-CE Recover Time	1	-	-	us
t_{PR}	VCC rising up time	0.1	100	-	ms
t_{PF}	VCC falling down time	3	300	-	ms
t_{W}(RESET)	Reset pulse width	10	-	-	ms
t_{H}(Hi-ZRESET)		0	-	-	
t_{S}(Hi-ZRESET)		0	-	-	

Figure 14: Timing Diagram, Hardware Reset



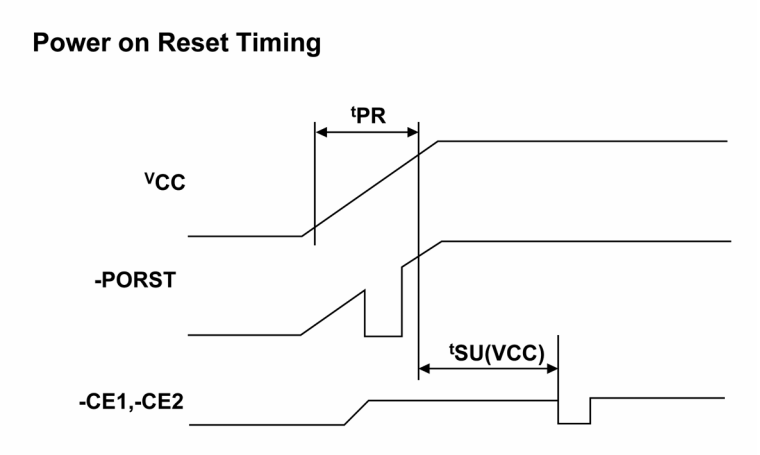
5.7 Power On Reset

When the VCC power reaches to 2.7V, the disk drive will be reset.

Table 18: Timing Diagram, Power On Reset

	Item	Min.	Max.	Normal	Unit	Note
t_{SU}(RESET)	-CE Setup Time	20	-	-	ms	
t_{PR}	-VCC Rising Up Time	0.1	100	-	ms	

Figure15: Timing Diagram, Power On Reset



6. Supported IDE Commands

iCF4000 supports the commands listed in Table 17.

Table 19: IDE Commands

Command Name	Command Code
Check Power Mode	98H or E5H
Execute Device Diagnostic	90H
Erase Sector	C0H
Format Track	50H
Identify Device	ECH
Idle	97H or E3H
Idle immediate	95H or E1H
Initialize Device Parameters	91H
NOP	00H
Read Buffer	E4H
Read DMA	C8H
Read Long Sector	22H or 23H
Read Multiple	C4H
Read Sector(s)	20H or 21H
Read Verify Sector(s)	40H or 41H
Recalibrate	1XH
Request Sense	03H
Security Disable Password	F6H
Security Erase Prepare	F3H
Security Erase Unit	F4H
Security Freeze Lock	F5h
Security Set Password	F1H
Security Unlock	F2H
Seek	7XH
Set Features	EFH
Set Multiple Mode	C6H
Set Sleep Mode	99H or E6H
Standby	96H or E2H
Standby Immediate	94H or E0H
Translate Sector	87H
Write Buffer	E8H
Write DMA	CAH

Write Long Sector	E8H
Write Multiple	C5H
Write Multiple without Erase	CDH
Write Sector(s)	30H or 31H
Write Sector(s) without Erase	38H
Write Verify	3CH

7. Device Parameters

iCF4000 device parameters listed in Table 18.

Table 20: Device parameters

Capacity	Total number of sectors	Cylinders	Heads	Sectors
32MB	64000	500	8	16
64MB	128000	500	8	32
128MB	256000	500	16	32
256MB	512000	1000	16	32
512MB	1023120	1015	16	63
1GB	2047248	2031	16	63
2GB	4095504	4063	16	63
4GB	8211168	8146	16	63
8GB	16128000	16000	16	63